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WHITE PAPER

Effective Monitoring, Test, and Repair of Multi-Die Designs

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Motivation for Multi-Die Designs

A multi-die semiconductor device is one in which multiple homogeneous or heterogeneous dies are contained within a single package. Multi-die technology has been available for select uses for years, but it is gaining broader adoption in a wide variety of end applications, including high-performance computing, artificial intelligence (AI), automotive, and mobile. There are two main factors driving the increased deployment of this technology.

The first trend is the disaggregation of large monolithic system-on-chip (SoC) devices into smaller dies (also referred to as chiplets). This trend is partly driven by technological factors, such as when large chips approach the reticle limits of semiconductor manufacturing equipment. Even when manufacturing a large monolithic die is feasible, yield may be limited such that it becomes more economical to fabricate multiple smaller dies. Disaggregation might apply to large central processing units (CPUs), graphics processing units (GPUs), or AI accelerators in application domains such as data centers, automotive, mobile, gaming, etc.

The second (counter) trend is aggregation, with the integration into one package of a set of discrete ICs previously sharing a printed circuit board (PCB). The die-to-die communication in a multi-die chip consumes much less power and provides significantly higher throughput compared to chip-to-chip communication over a PCB. Multi-die integration is common in the networking domain, combining digital chips and co-packaged optics.

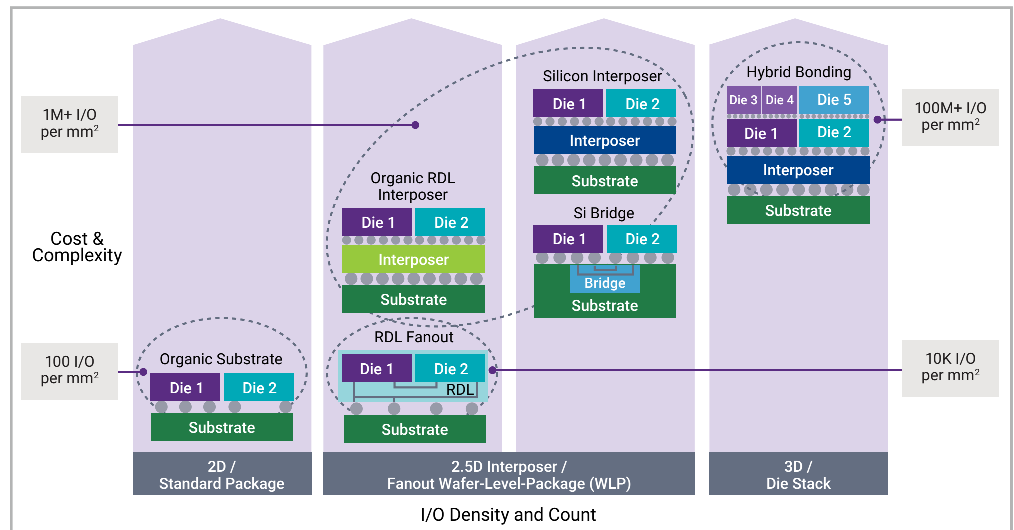

Figure 1: Types of packaging technologies for multi-die designs and achievable I/O density

For both disaggregation and aggregation, there are several compelling advantages to multi-die designs. As shown in Figure 1, much higher I/O densities are achievable, helping to increase throughput. Products can be assembled much more quickly from existing parts, especially variants targeted for specific applications, enabling a more flexible solutions portfolio. Multi-die designs shorten time-to-market (TTM) while reducing project risk by reusing existing, proven dies. This is particularly beneficial when aggregating components such as analog blocks that will otherwise not benefit from implementation on advanced and expensive manufacturing nodes.

Challenges in Testing Multi-Die Designs

Despite clear advantages, the decision to design a multi-die chip rather than a traditional monolithic SoC is not easy. There are new challenges that need to be addressed for successful multi-die realization, as shown in Figure 2. This white paper focuses on the multi-die test challenges, including:

- Bare chiplet level (pre-bond)
  - Probe, dedicated/functional pads for test
  - Test, diagnosis, and repair
- Interconnects (mid/post-bond)
  - Die-to-die test access
  - Lane test, diagnosis, and repair
- Multi-die stack/package (post-bond)
  - Die-to-die, stack/package test access
  - Calibration, diagnosis, and repair
  - Silicon debug and diagnosis

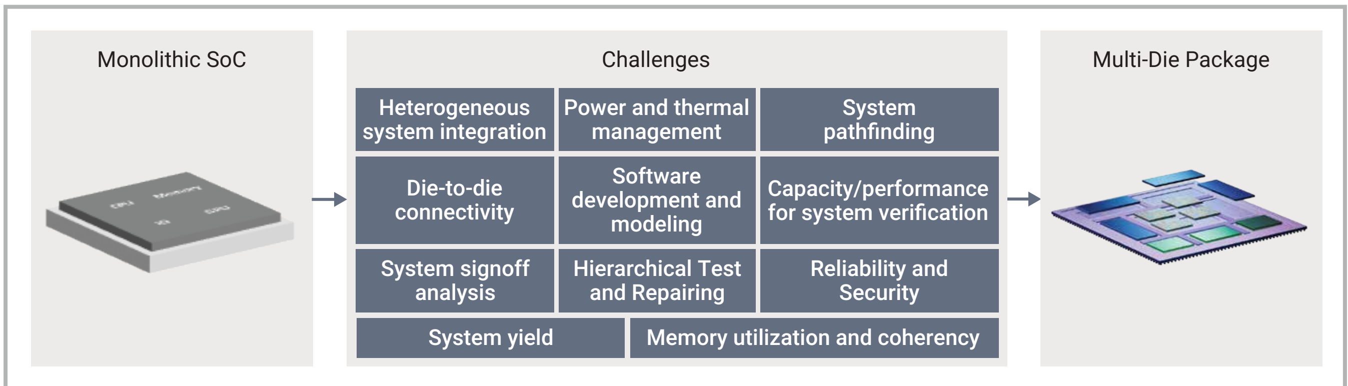

Figure 2: Multi-die design challenges

These challenges go beyond the design phase, covering both manufacturing and deployment in the field. In fact, support for multi-die test, monitor, and repair must span the entire scope of the silicon lifecycle. Methods and standards must provide access for monitoring resources as well as test and repair of both dies and assemblies. These must handle:

- High-speed logic-to-memory interfaces such as High Bandwidth Memory (HBM)
- Logic-to-logic interfaces, both high speed physical layer (PHY) such as Universal Chiplet Interconnect Express (UCIe) and low speed non-PHY

Analytics are required at every stage of the silicon lifecycle: in-design, in-ramp, in-production, and in-field. The goal is to ensure multi-die quality, reliability, and yield.

The Synopsys Multi-Die Test Solution

Multi-die designs are more costly to build and test than traditional single-die packages. Only one failed die in a multi-die configuration can cause the entire system to fail. Thus, the quality of each die and the integrity of the interconnect is critical. Experiencing late-stage failures can be catastrophic if not resolved quickly. Any effective solution mandates the use of a co-design platform, backed by several techniques and established standards. Figure 3 shows the key elements in the Synopsys multi-die test, monitor, and repair solution.

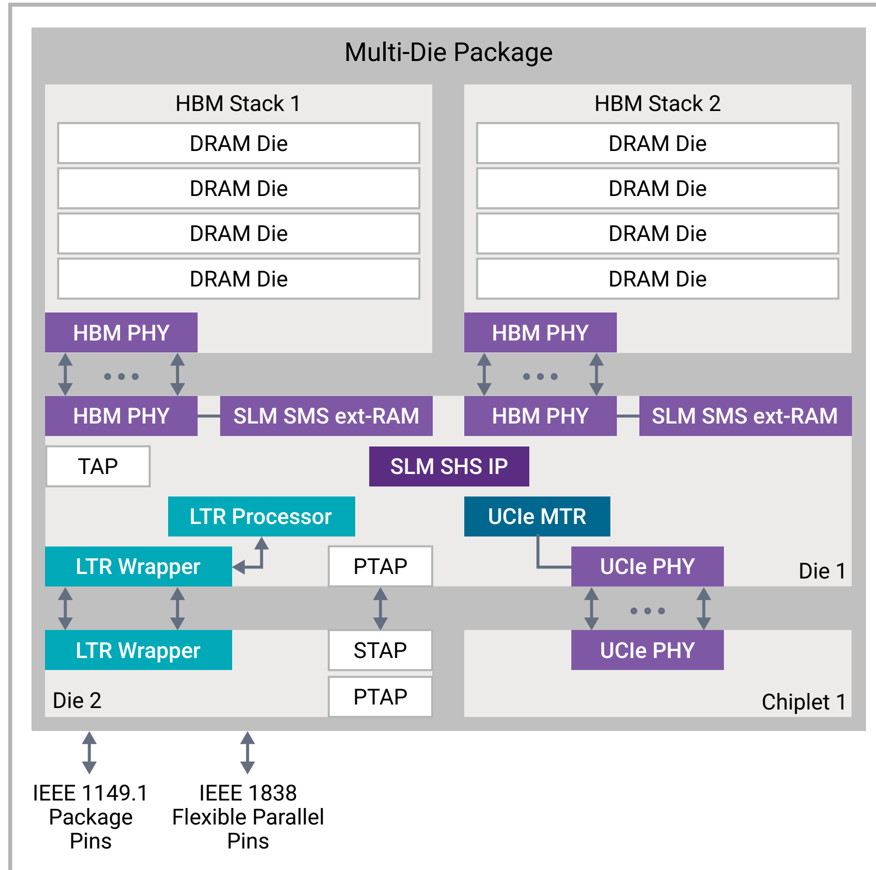

Figure 3: Elements of a multi-die test solution

The Synopsys solution for multi-die testability can handle all types of die-to-die interfaces:

- Logic-to-logic interfaces
  - Non-PHY based interfaces
    - Regular/low speed I/O based interfaces
    - High speed/high volume interfaces that feature redundancy
  - High speed PHY-to-PHY based interfaces such as UCIe
- High speed logic-to-memory interfaces such as HBM

For manufacturing, all aspects of intra-die, inter-die, and package level testing can be accomplished during the pre-bond, mid-bond and post-bonding stages. Synopsys offers a DFx solution that includes automated design for test (DFT) insertion with die-to-die and stack level access, die-to-die interconnect pattern generation with identification of faults, pattern porting for die-to-die and stack level, multi-die diagnosis and traceability as well as monitoring in-system for purposes such as predictive maintenance.

Synopsys Silicon Lifecycle Management (SLM) solution provides testability to cover all phases of the design: in-design, in-ramp, in-production, and in-field.

Synopsys Solutions for IEEE1838 and Lane Test and Repair (LTR)

The IEEE 1838 Standard for *Test Access Architecture for Three-Dimensional Stacked Integrated Circuits* provides the key DFT access architecture. This standard supports test of both individual dies and die-to-die interconnects. It is intended for low speed/low volume lanes.

IEEE 1838 is a die-centric standard, applying to a die that is intended to be part of a multi-die design and defining die-level features. When compliant dies are combined into a stacked configuration, these features form a stack-level architecture for test of both intra-die circuitry and inter-die connections. It supports individual dies, partial stacks, and complete stacks, thus spanning pre-packaging, post-packaging, and board-level stages. Interconnects supported include through-silicon vias (TSVs), wire bonding, and other technologies.

Figure 4 presents a high-level view of the IEEE 1838 DFT architecture applied to a multi-die design. It includes the use of the Synopsys SLM SHS IP automated hierarchical test solution.

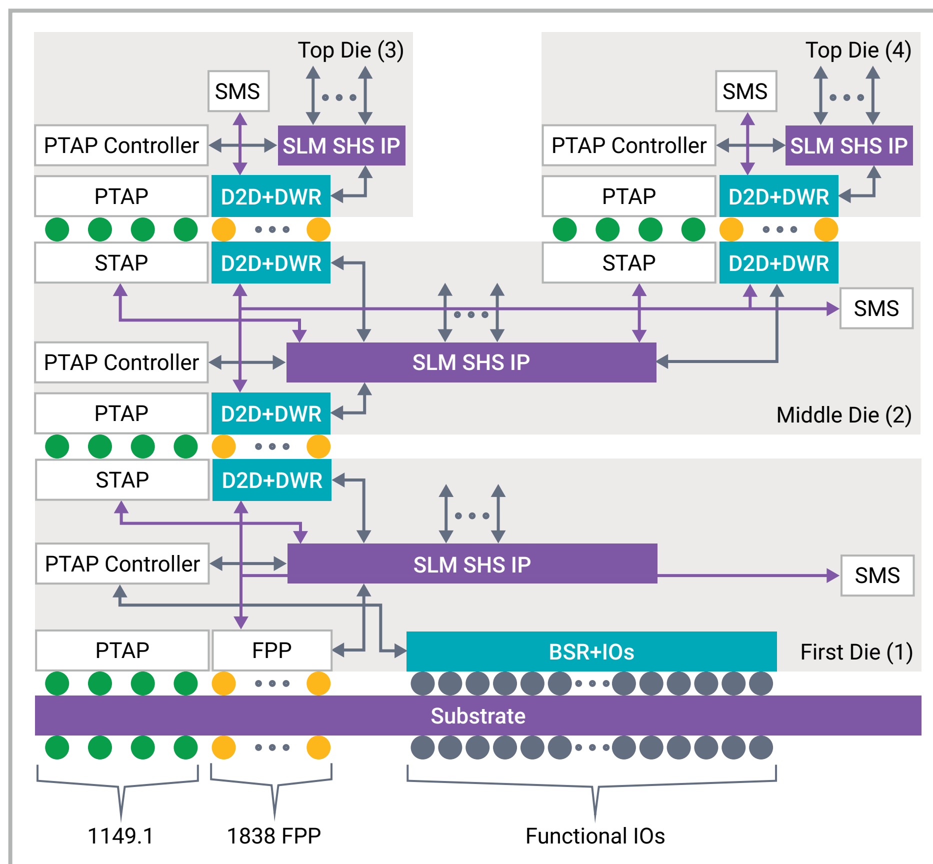

Figure 4: IEEE 1838 DFT architecture with Hierarchical SLM SHS IP Fabric and FPP

Key components of the architecture shown in Figure 4 include:

- Hierarchical SHS Fabric
  - SLM SHS IP network on each die supports internal and die-to-die test
  - Supports IEEE 1149.1, IEEE 1500. and IEEE 1687
- SLM SMS IP and Scan Fabric
  - Supports memory test and repair, and parallel scan for compression and logic BIST
- Primary Test Access Port (PTAP)
  - PTAP Controller is a TAP controller with instructions for SHS access

- Secondary Test Access Port (STAP)
  – IEEE 1149.1 port to interface with next/subsequent die
- Die Wrapper Register (DWR)
  – Die-to-die interconnect test between PHYs
- 1149.1 Boundary Scan Register (BSR) for the package
  – Functional package I/Os and BSR are on the first die
- Flexible Parallel Port (FPP)
  – Optional, scalable multi-bit test access mechanism that offers higher test access bandwidth than the mandatory one-bit serial port

Synopsys offers an LTR approach which provides system-level built-in self-test (BIST) for high-volume lanes in die-to-die interconnections. It supports reconfiguration and repair using redundant lanes. The IEEE 1149.1 Standard for *Test Access Port and Boundary-Scan Architecture* and its Test Access Port (TAP) controller remain relevant to this architecture solution.

LTR is required to prevent system failure due to faulty die-to-die lanes, which could otherwise occur due to coupling faults (as an example). To achieve high test coverage, it is important to detect these types of faults at speed. Figure 5 shows an example of this technique in action. A faulty lane has been detected by die-to-die test, so signals are shifted from the faulty lane to a spare lane. The same lane shift is implemented for the dies on both sides of the interconnect. The faulty lane output I/O is placed into standby mode.

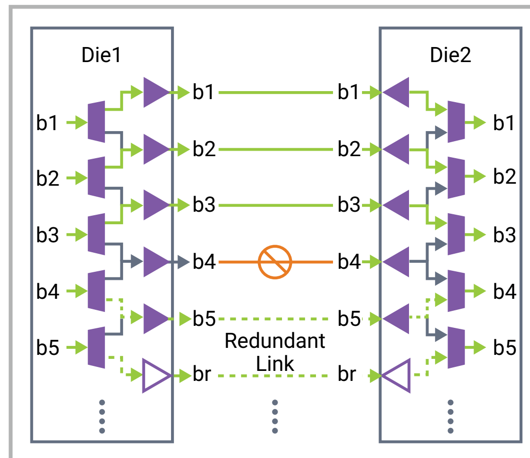

Figure 5: Faulty lane remapping with LTR

Synopsys ext-RAM and UCIe Monitor, Test, and Repair (MTR) IP

The architecture defined in the previous section supports die-to-die test, including logic to logic and logic to memory. Dies are tested individually before packaging, external memory and interconnects are tested, and the TAP controllers are used to run tests after packaging. However, there are two more key technologies needed for a complete multi-die test solution.

The HBM standard defines an interface for 3D-stacked synchronous dynamic random-access memory (DRAM) dies. It specifies the PHY-level logic-to-memory interconnection. Synopsys SLM SMS ext-RAM IP supports at-speed interconnect test and diagnosis of memory dies as well as post package repair (PPR).

This IP provides:

- Comprehensive at-speed interface and memory array testing and diagnosis
- Programmable test algorithms, address types and ranges, test operation time, and DRAM access timing
- Diagnostics data reporting
- Memory fault type and failing address/data lanes
- Post-packaging repair via HBM stack repair signature

Figure 6 shows how the Synopsys SLM SMS ext-RAM IP interconnects with the memory controller, the memory PHY, and the memory stack, using the HBM3 standard.

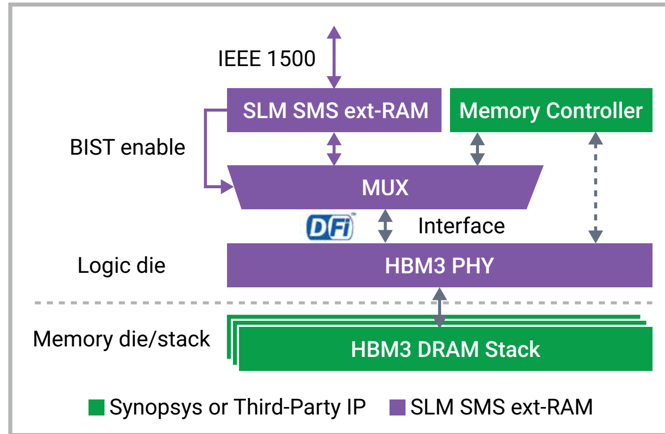

Figure 6: Synopsys SLM SMS ext-RAM IP for memory test and repair

The UCIe is an increasingly widely adopted PHY standard for die-to-die connectivity. Despite its popularity, UCIe presents challenges for effective SLM. Traditional probing is challenging for the bump pitch of current and emerging packages, so a built-in approach is required. Such a solution cannot mandate additional DFT signals beyond the mainband and sideband connections defined by the UCIe standard. The solution must provide high interconnect defect/fault coverage, loopback test, incremental multi-corner test in manufacturing, and in-field detection of aging/degradation effects.

The Synopsys UCIe MTR IP is a necessary component of a multi-die test solution. It supports the full range of SLM for multi-die designs where UCIe is the primary interconnect mechanism. Synopsys UCIe MTR IP, intended for Synopsys UCIe type PHYs, performs the critical monitoring, test, and repair functionality. It provides two-lane remapping as well as one-lane remapping. It supports both hard repair and incremental soft repair when lane failures are not permanent. It can initiate lane repair logic test, near-end and far-end loopback BIST, and PHY die-to-die BIST. There is support for PHY initialization (low-speed test) and training (high-speed test) as well as eye monitoring via the Signal Integrity Monitor (SIM) embedded into the Synopsys PHY. It manages repair and hierarchical SLM at the multi-die level, for a comprehensive and scalable solution. Figure 7 shows an example of Synopsys UCIe MTR deployed in a die-to-die interconnect using UCIe.

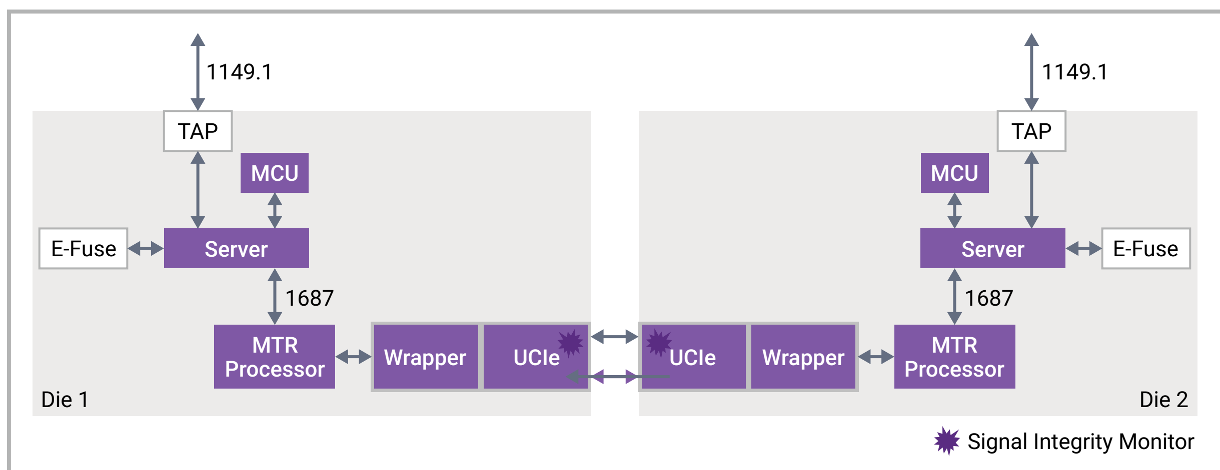

Figure 7: Synopsys SLM UCIe MTR IP for monitoring, test, and repair

Summary

The growing importance of multi-die designs highlights the challenges associated with monitoring, testing and repair of packaged parts. Traditional probe-based methods cannot meet the demands. A solution must not only meet these challenges, but also span the full silicon lifecycle. Required DFx features must include test and repair of different types of die-to-die interfaces, perform lane test and repair, test for and diagnose known-good stack and known-good die, support extensive BIST capabilities, and offer in-field interconnect monitoring for purposes such as predictive maintenance. Synopsys provides a comprehensive and scalable solution for multi-die monitor, test, and repair.

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